IXDD504/ IXDE504

4 Ampere Dual Low-Side Ultrafast MOSFET Drivers with Enable for fast, controlled shutdown

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected up to 4 Amps
- High 4A Peak Output Current
- Wide Operating Range: 4.5V to 30V
- -55°C to +125°C Extended Operating Temperature
- Ability to Disable Output under Faults
- High Capacitive Load Drive Capability: 1800pF in <15ns
- Matched Rise And Fall Times
- Low Propagation Delay Time
- Low Output Impedance
- Low Supply Current
- Two Drivers in a Single Package

Applications

- Limiting di/dt under Short Circuit
- Driving MOSFETs and IGBTs
- Motor Controls
- Line Drivers
- Pulse Generators
- Local Power ON/OFF Switch
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Pulse Transformer Driver
- Class D Switching Amplifiers
- Power Charge Pumps

General Description

The IXDD504 and IXDE504 each consist of two 4-Amp CMOS high speed MOSFET gate drivers for driving the latest IXYS MOSFETs & IGBTs. Each of the dual outputs can source and sink 4 Amps of peak current while producing voltage rise and fall times of less than 15ns. The input of each driver is TTL or CMOS compatible and is virtually immune to latch up. Patented* design innovations eliminate cross conduction and current "shoot-through". Improved speed and drive capabilities are further enhanced by fast, matched rise and fall times.

Additionally, each IXDD504 or IXDE504 driver incorporates a unique ability to disable the output under fault conditions. When a logical low is forced into the Enable input of a driver, both of it's final output stage MOSFETs (NMOS and PMOS) are turned off. As a result, the respective output of the IXDD504 enters a tristate mode and, with additional cicuitry, achieves a soft turn-off of the MOSFET/IGBT when a short circuit is detected. This helps prevent damage that could occur to the MOSFET/IGBT if it were to be switched off abruptly due to a dv/dt over-voltage transient.

The IXDD504 and IXDE504 are each available in the 8-Pin P-DIP (PI) package, the 8-Pin SOIC (SIA) package, and the 8-Lead DFN (D2) package, (which occupies less than 65% of the board area of the 8-Pin SOIC).

*United States Patent 6,917,227

Ordering Information

Part Number	Description	Package Type	Packing Style	Pack Qty	Configuration
IXDD504PI	4A Low Side Gate Driver I.C.	8-Pin PDIP	Tube	50	Dual Non-Inverting Drivers with Enable
IXDD504SIA	4A Low Side Gate Driver I.C.	8-Pin SOIC	Tube	94	
IXDD504SIAT/R	4A Low Side Gate Driver I.C.	8-Pin SOIC	13” Tape and Reel	2500	
IXDD504D2	4A Low Side Gate Driver I.C.	8-Lead DFN	2” x 2” Waffle Pack	56	
IXDD504D2T/R	4A Low Side Gate Driver I.C.	8-Lead DFN	13” Tape and Reel	2500	
IXDE504PI	4A Low Side Gate Driver I.C.	8-Pin PDIP	Tube	50	Dual Inverting Drivers Inverting with Enable
IXDE504SIA	4A Low Side Gate Driver I.C.	8-Pin SOIC	Tube	94	
IXDE504SIAT/R	4A Low Side Gate Driver I.C.	8-Pin SOIC	13” Tape and Reel	2500	
IXDE504D2	4A Low Side Gate Driver I.C.	8-Lead DFN	2” x 2” Waffle Pack	56	
IXDE504D2T/R	4A Low Side Gate Driver I.C.	8-Lead DFN	13” Tape and Reel	2500	

NOTE: All parts are lead-free and RoHS Compliant

Figure 1 - IXDD504 Dual Non-Inverting + Enable 4A Gate Driver Functional Block Diagram

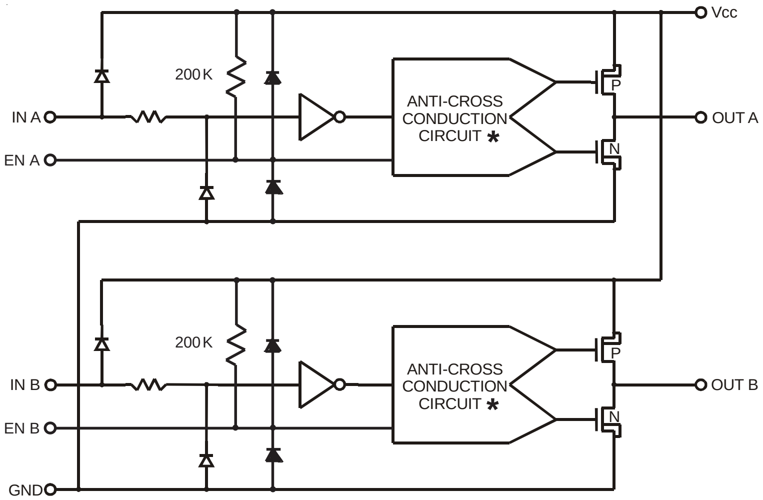
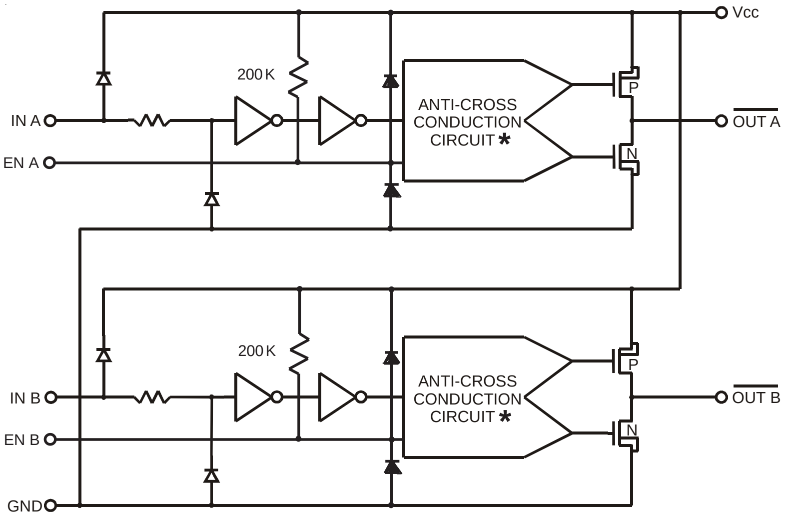


Figure 2 - IXDE504 Dual Inverting + Enable 4A Gate Driver Functional Block Diagram



---

* **United States Patent 6,917,227**

Absolute Maximum Ratings [1]

Parameter	Value
Supply Voltage	35 V
All Other Pins (unless specified otherwise)	-0.3 V to V_{CC} + 0.3V
Junction Temperature	150 °C
Storage Temperature	-65 °C to 150 °C
Lead Temperature (10 Sec)	300 °C

Operating Ratings [2]

Parameter	Value
Operating Supply Voltage	4.5V to 30V
Operating Temperature Range	-55 °C to 125 °C

Package Thermal Resistance*			
8-Pin PDIP	(PI)	θ_{J-A} (typ)	125 °C/W
8-Pin SOIC	(SIA)	θ_{J-A}(typ)	200 °C/W
8-Lead DFN	(D2)	θ_{J-A}(typ)	125-200 °C/W
8-Lead DFN	(D2)	θ_{J-C}(max)	2.1 °C/W
8-Lead DFN	(D2)	θ_{J-S}(typ)	6.4 °C/W

Electrical Characteristics @ T_A = 25 °C [3]

Unless otherwise noted, 4.5V ≤ V_{CC} ≤ 30V .

All voltage measurements with respect to GND. IXD_504 configured as described in *Test Conditions*. All specifications are for one channel.

Symbol	Parameter	Test Conditions	Min	Typ [4]	Max	Units
V_{IH}, V_{ENH}	High input & EN voltage	4.5V ≤ V_{IN} ≤ 18V	3			V
V_{IL}, V_{ENL}	Low input & EN voltage	4.5V ≤ V_{IN} ≤ 18V			0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
V_{EN}	Enable voltage range		- 0.3		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	High state output resistance	V_{CC} = 18V I_{OUT} = 10mA		1.5	2.5	Ω
R_{OL}	Low state output resistance	V_{CC} = 18V I_{OUT} = 10mA		1.2	2.0	Ω
I_{PEAK}	Peak output current	V_{CC} = 15V		4		A
I_{DC}	Continuous output current	Limited by package dissipation			1	A
t_R	Rise time	C_{LOAD} =1000pF V_{CC} =18V		9	16	ns
t_F	Fall time	C_{LOAD} =1000pF V_{CC} =18V		8	14	ns
t_{ONDLY}	On-time propagation delay	C_{LOAD} =1000pF V_{CC} =18V		19	40	ns
t_{OFFDLY}	Off-time propagation delay	C_{LOAD} =1000pF V_{CC} =18V		18	35	ns
t_{ENOH}	Enable to output high delay time			15	30	ns
t_{DOLD}	Disable to high impedance state delay time			63	100	ns
V_{CC}	Power supply voltage		4.5	18	30	V
R_{EN}	Enable Pull-up Resistor			200		kΩ
I_{CC}	Power supply current	V_{CC} = 18V, V_{IN} = 0V V_{IN} = 3.5V V_{IN} = V_{CC}		1	20 3 20	µA mA mA

Electrical Characteristics @ temperatures over -55 ºC to 125 ºC (3)

Unless otherwise noted, $4.5V \le V_{CC} \le 30V$, Tj < 150ºC

All voltage measurements with respect to GND. IXD_504 configured as described in *Test Conditions*. All specifications are for one channel.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage	$4.5V \le V_{CC} \le 18V$	3			V
V_{IL}	Low input voltage	$4.5V \le V_{CC} \le 18V$			0.8	V
V_{IN}	Input voltage range		-5		$V_{CC} + 0.3$	V
I_{IN}	Input current	$0V \le V_{IN} \le V_{CC}$	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	High state output resistance	$V_{CC} = 18V$, $I_{OUT} = 10mA$			3	Ω
R_{OL}	Low state output resistance	$V_{CC} = 18V$, $I_{OUT} = 10mA$			2.5	Ω
I_{DC}	Continuous output current				1	A
t_R	Rise time	C_{LOAD} =1000pF V_{CC} =18V			10	ns
t_F	Fall time	C_{LOAD} =1000pF V_{CC} =18V			9	ns
t_{ONDLY}	On-time propagation delay	C_{LOAD} =1000pF V_{CC} =18V			23	ns
t_{OFFDLY}	Off-time propagation delay	C_{LOAD} =1000pF V_{CC} =18V			32	ns
t_{ENOH}	Enable to output high delay time				60	ns
t_{DOLD}	Disable to high impedance state delay time				120	ns
V_{CC}	Power supply voltage		4.5	18	30	V
I_{HIOL}	High impedance state output leakage	V_{CC} = 18V, Temp. = 125°C			200	µA
I_{CC}	Power supply current	$V_{CC} = 18V$, $V_{IN} = 0V$ $V_{IN} = 3.5V$ $V_{IN} = V_{CC}$			150 3 150	µA mA mA

Notes:

1. Operating the device beyond the parameters listed as “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The device is not intended to be operated outside of the Operating Ratings.
3. Electrical Characteristics provided are associated with the stated Test Conditions.
4. Typical values are presented in order to communicate how the device is expected to perform, but not necessarily to highlight any specific performance limits within which the device is guaranteed to function.

* The following notes are meant to define the conditions for the θ_{J-A}, θ_{J-C} and θ_{J-S} values:

1) The θ_{J-A} (typ) is defined as junction to ambient. The θ_{J-A} of the standard single die 8-Lead PDIP and 8-Lead SOIC are dominated by the resistance of the package, and the IXD_5XX are typical. The values for these packages are natural convection values with vertical boards and the values would be lower with forced convection. For the 8-Lead DFN package, the θ_{J-A} value supposes the DFN package is soldered on a PCB. The θ_{J-A} (typ) is 200 °C/W with no special provisions on the PCB, but because the center pad provides a low thermal resistance to the die, it is easy to reduce the θ_{J-A} by adding connected copper pads or traces on the PCB. These can reduce the θ_{J-A} (typ) to 125 °C/W easily, and potentially even lower. The θ_{J-A} for DFN on PCB without heatsink or thermal management will vary significantly with size, construction, layout, materials, etc. This typical range tells the user what he is likely to get if he does no thermal management.

2) θ_{J-C} (max) is defined as juction to case, where case is the large pad on the back of the DFN package. The θ_{J-C} values are generally not published for the PDIP and SOIC packages. The θ_{J-C} for the DFN packages are important to show the low thermal resistance from junction to the die attach pad on the back of the DFN, -- and a guardband has been added to be safe.

3) The θ_{J-S} (typ) is defined as junction to heatsink, where the DFN package is soldered to a thermal substrate that is mounted on a heatsink. The value must be typical because there are a variety of thermal substrates. This value was calculated based on easily available IMS in the U.S. or Europe, and not a premium Japanese IMS. A 4 mil dialectric with a thermal conductivity of 2.2W/mC was assumed. The result was given as typical, and indicates what a user would expect on a typical IMS substrate, and shows the potential low thermal resistance for the DFN package.

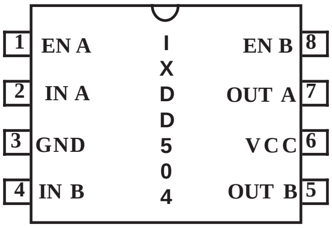
Pin Description

SYMBOL	FUNCTION	DESCRIPTION
EN A	A Channel Enable	Channel A enable pin. When driven low, this pin disables the A channel and forces a high impedance state to the A channel output.
IN A	A Channel Input	A channel input signal-TTL or CMOS compatible.
GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.
IN B	B Channel Input	B channel input signal-TTL or CMOS compatible.
OUT B	B Channel Output	B channel driver output. For application purposes, this pin is connected via a resistor to the gate of a MOSFET/IGBT.
VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 4.5V to 30V.
OUT A	A Channel Output	A channel driver output. For application purposes, this pin is connected via a resistor to the gate of a MOSFET/IGBT.
EN B	B Channel Enable	Channel B enable pin. When driven low, this pin disables the B channel and forces a high impedance state to the B channel output.

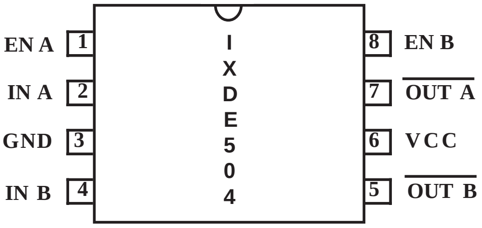
CAUTION: Follow proper ESD procedures when handling and assembling this component.

Pin Configurations

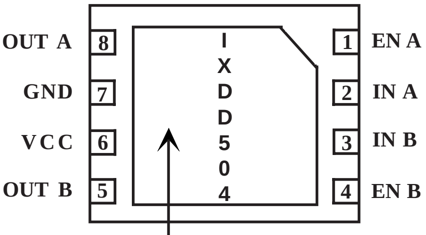
8 PIN DIP (PI)
8 PIN SOIC (SIA)



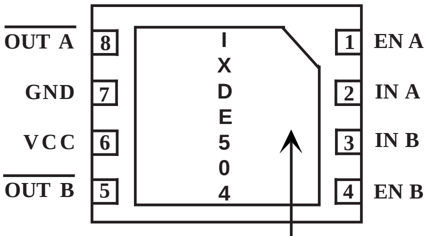
8 PIN DIP (PI)
8 PIN SOIC (SIA)



8 LEAD DFN (D2)
(Bottom View)

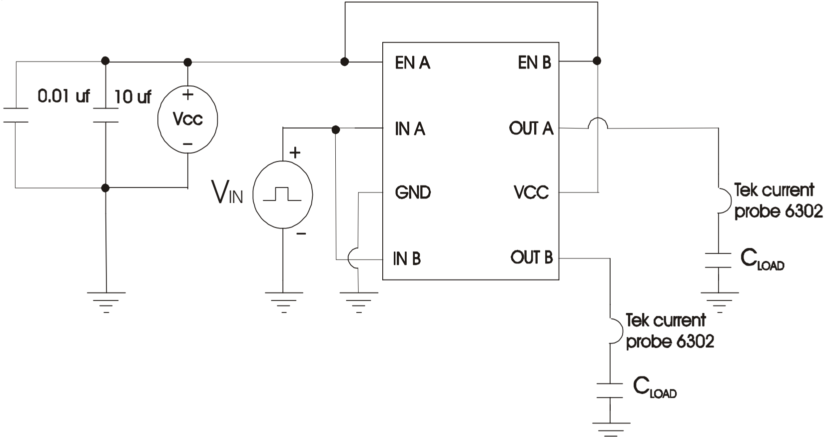


8 LEAD DFN (D2)
(Bottom View)



NOTE: Solder tabs on bottoms of DFN packages are grounded

Figure 3 - Characteristics Test Diagram



Typical Performance Characteristics

Fig. 4

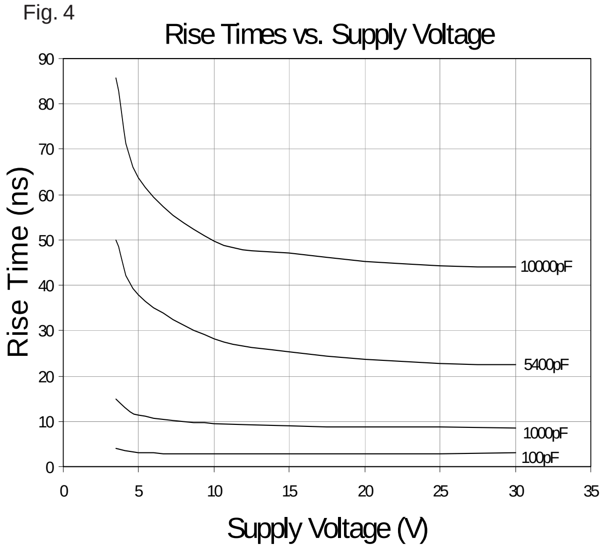

Rise Times vs. Supply Voltage

Fig. 5

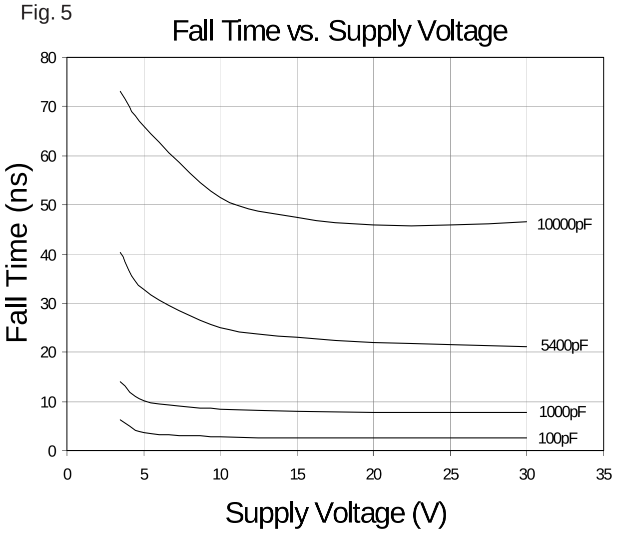
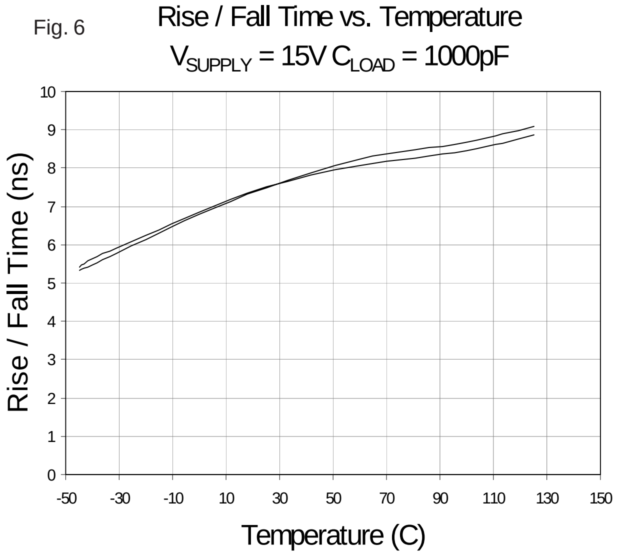

Fall Time vs. Supply Voltage

Fig. 6


Rise / Fall Time vs. Temperature

V_{SUPPLY} = 15V C_{LOAD} = 1000pF

Fig. 7

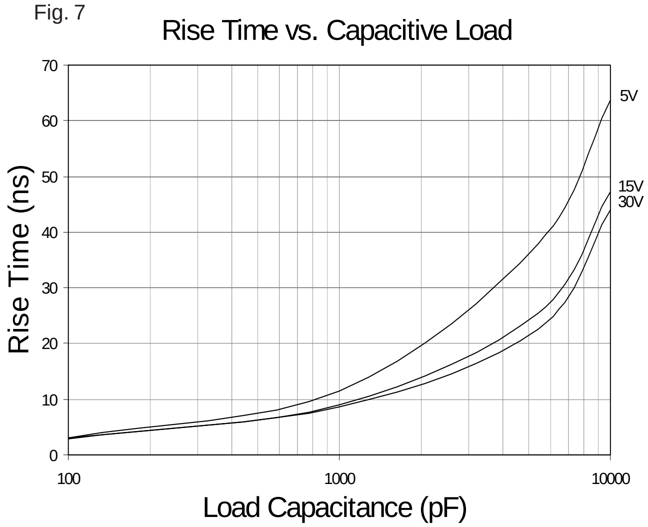

Rise Time vs. Capacitive Load

Fig. 8

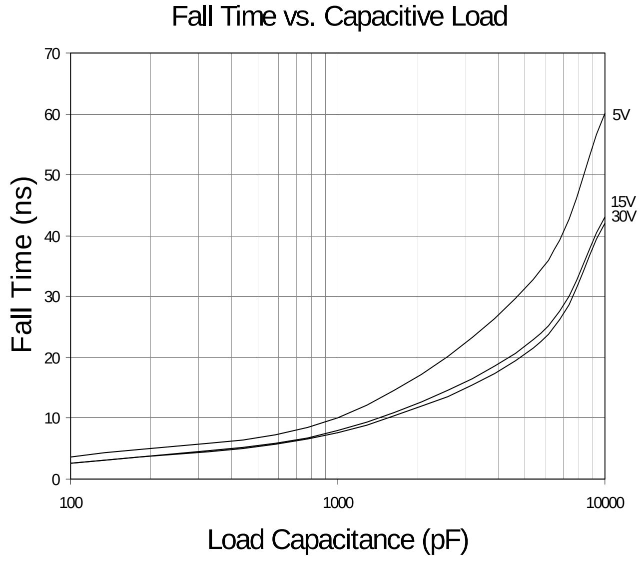

Fall Time vs. Capacitive Load

Fig. 9

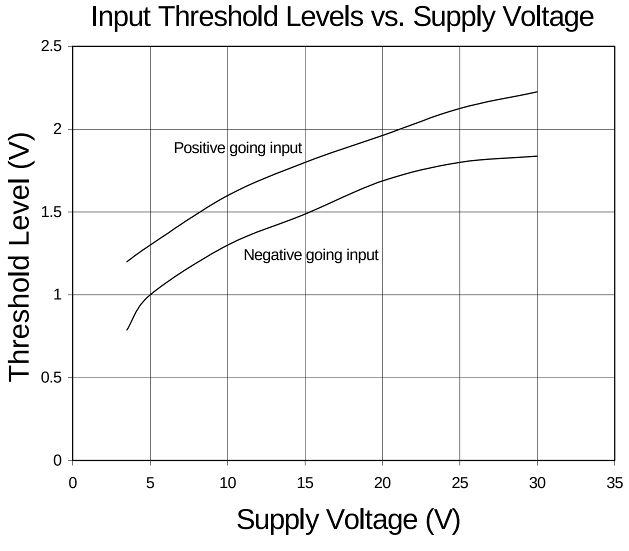

Input Threshold Levels vs. Supply Voltage

Fig. 10

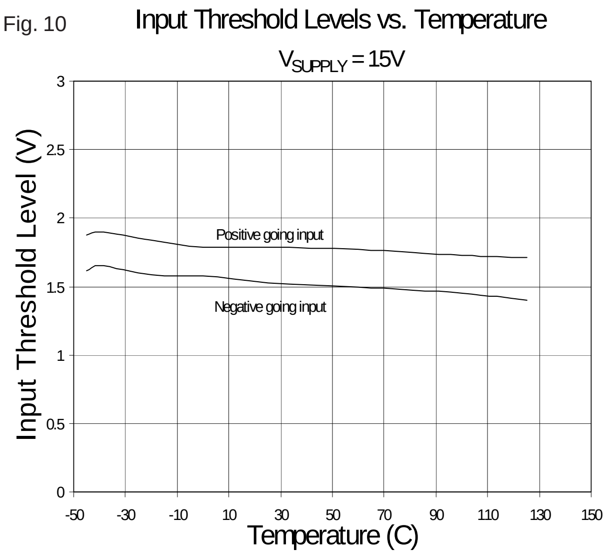


Fig. 11

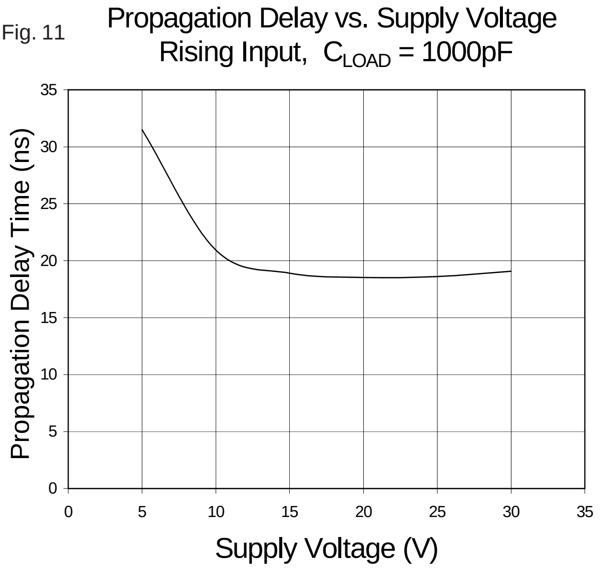


Fig. 12

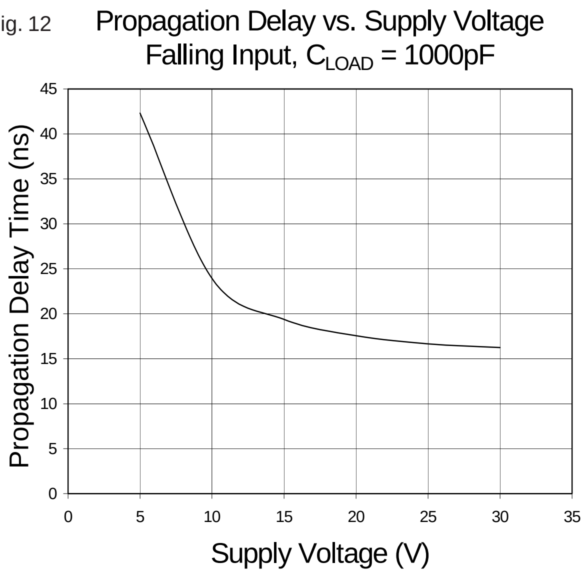


Fig. 13

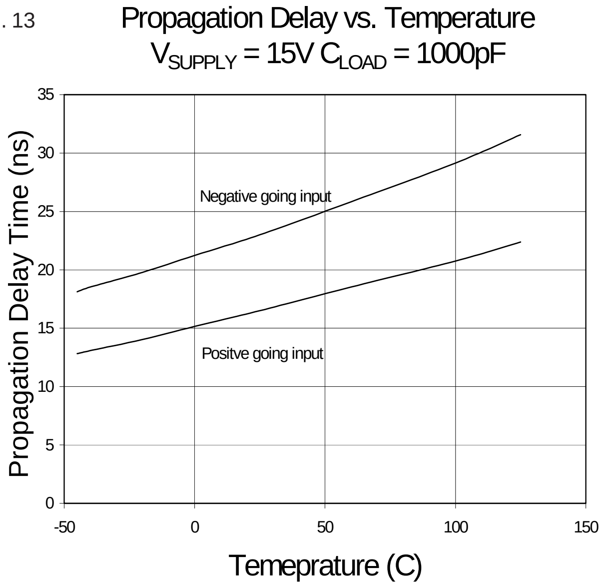


Fig. 14

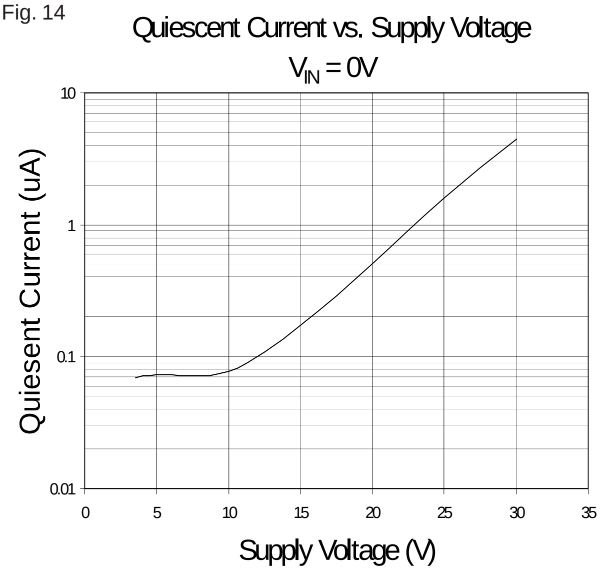


Fig. 15

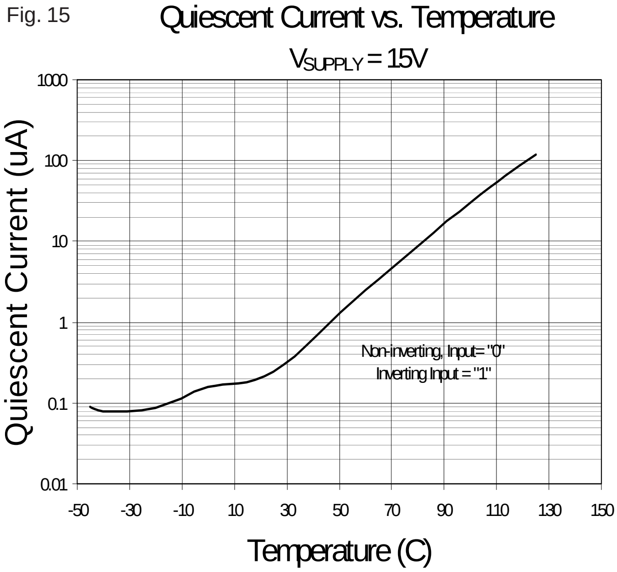


Fig. 16

Supply Current vs. Capacitive Load $V_{SUPPLY} = 5V$

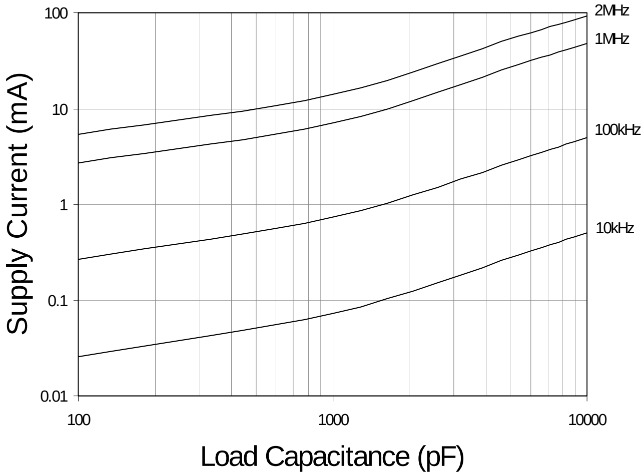


Fig. 17

Supply Current vs. Frequency $V_{SUPPLY} = 5V$

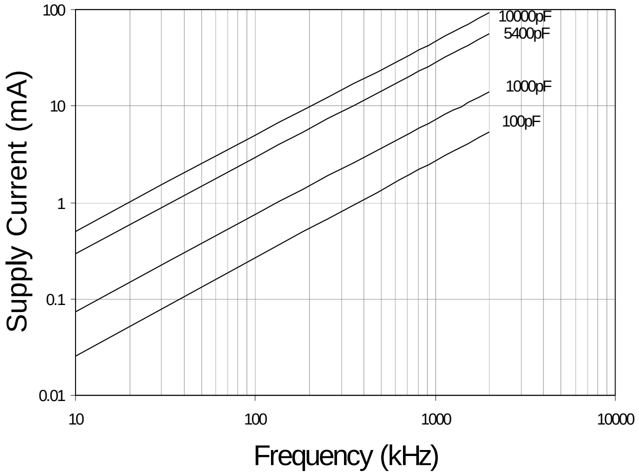


Fig. 18

Supply Current vs. Capacitive Load $V_{SUPPLY} = 15V$

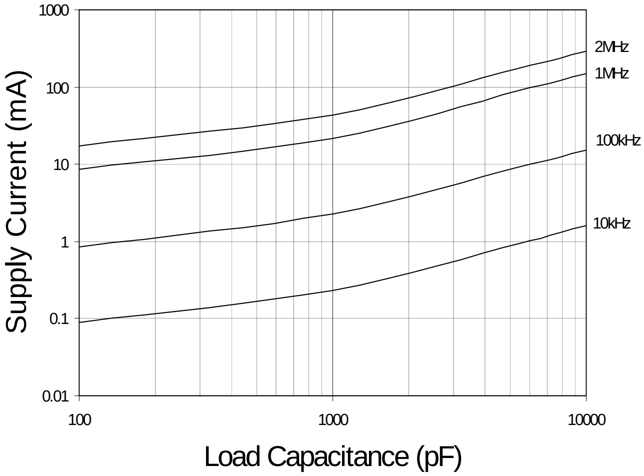


Fig. 19

Supply Current vs. Frequency $V_{SUPPLY} = 15V$

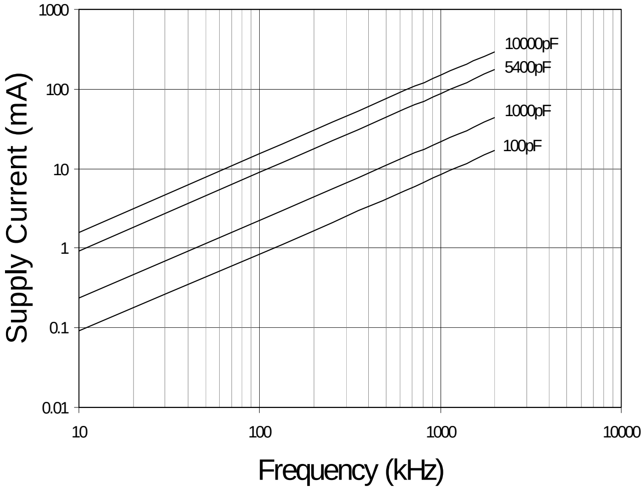


Fig. 20

Supply Current vs. Capacitive Load $V_{SUPPLY} = 30V$

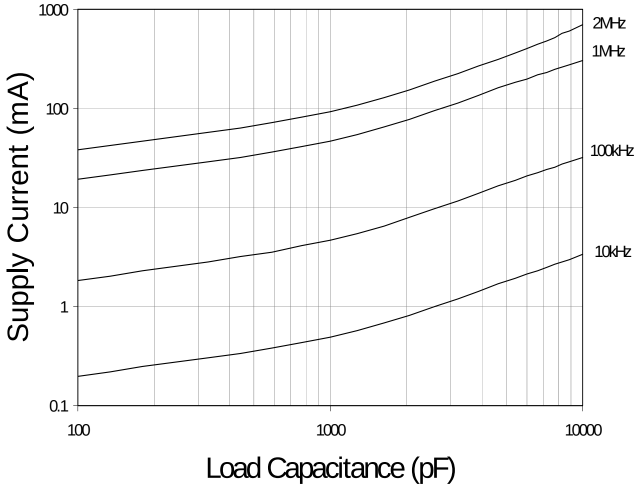


Fig. 21

Supply Current vs. Frequency $V_{SUPPLY} = 30V$

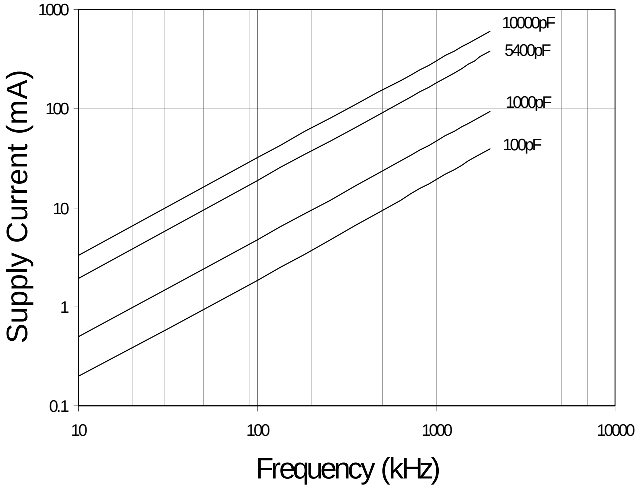


Fig. 22

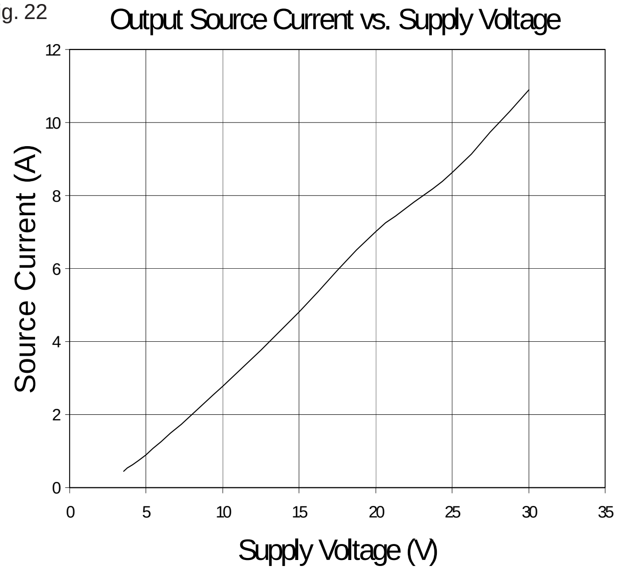


Fig. 23

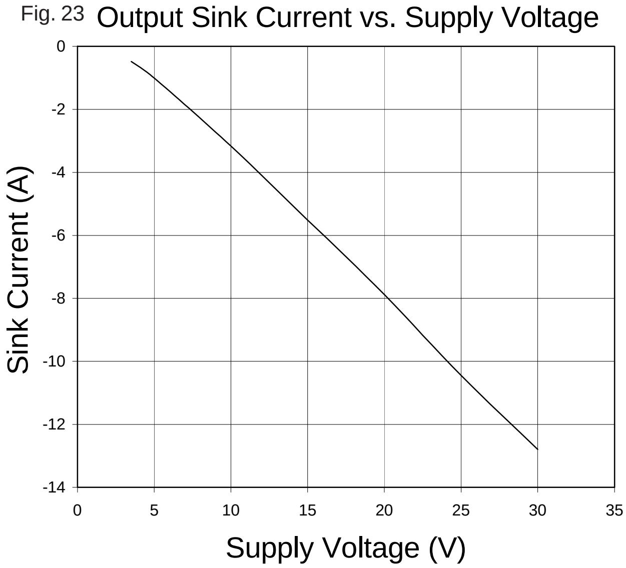


Fig. 24

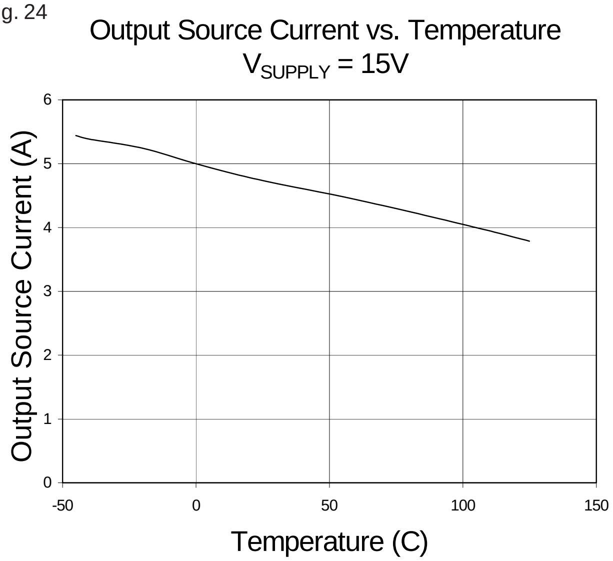


Fig. 25

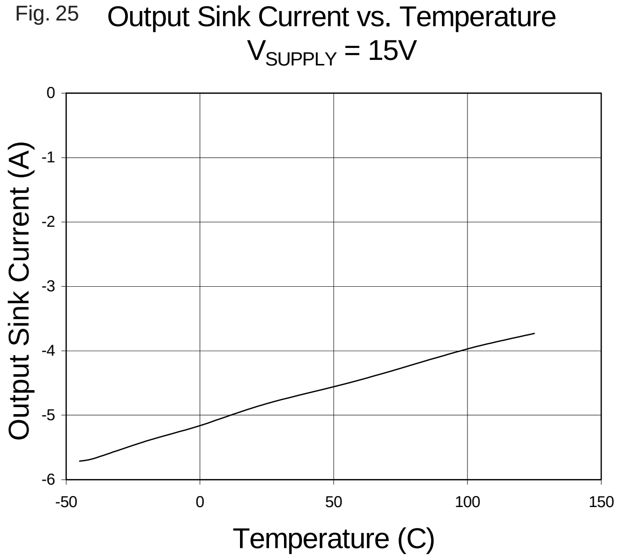


Fig. 26

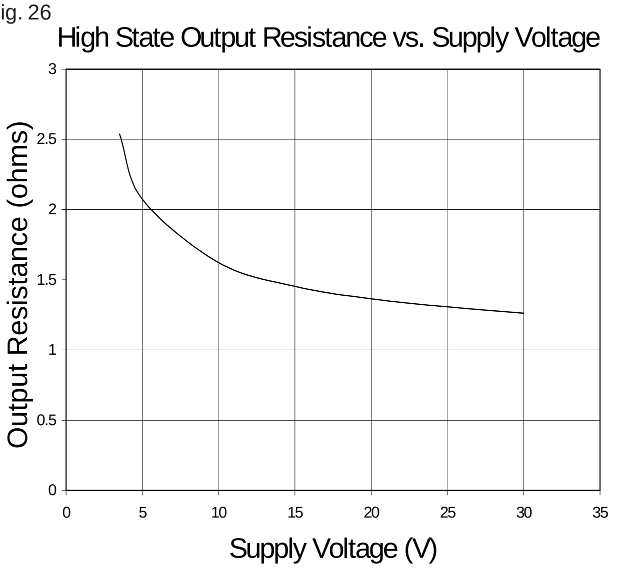


Fig. 27

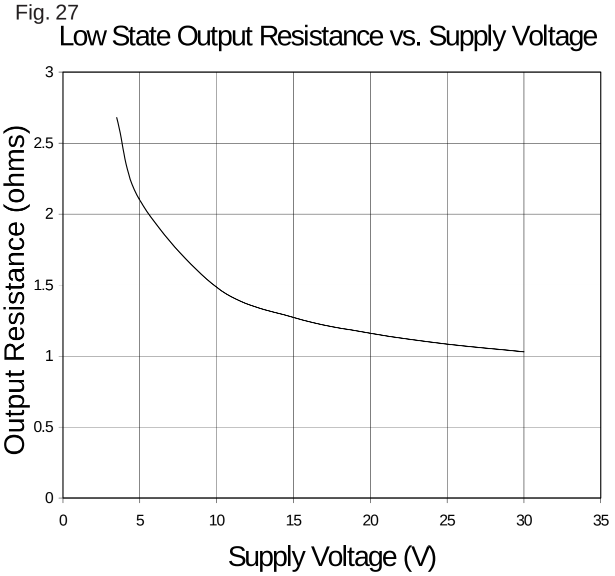


Fig. 28

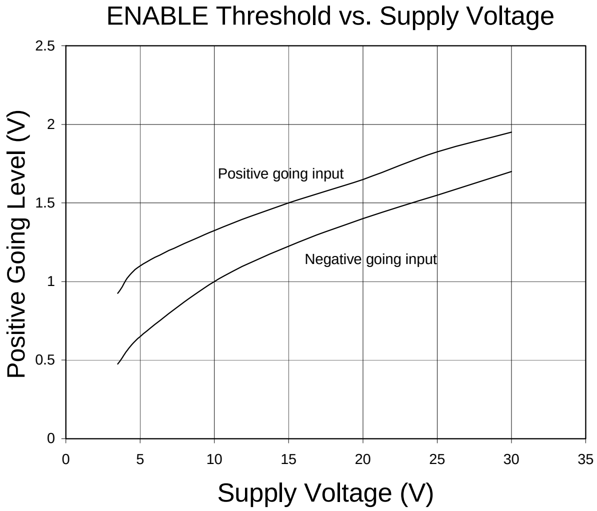


Fig. 29

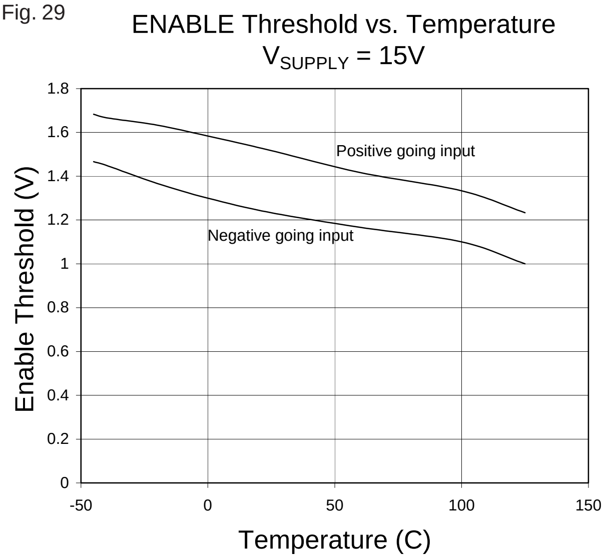


Fig. 30

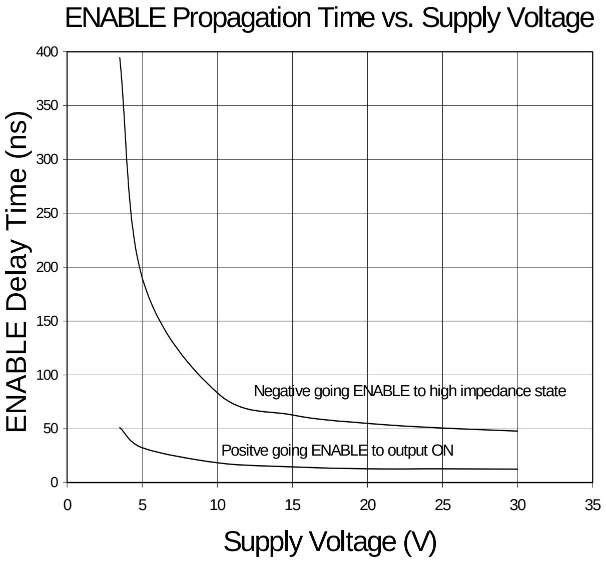


Fig. 31

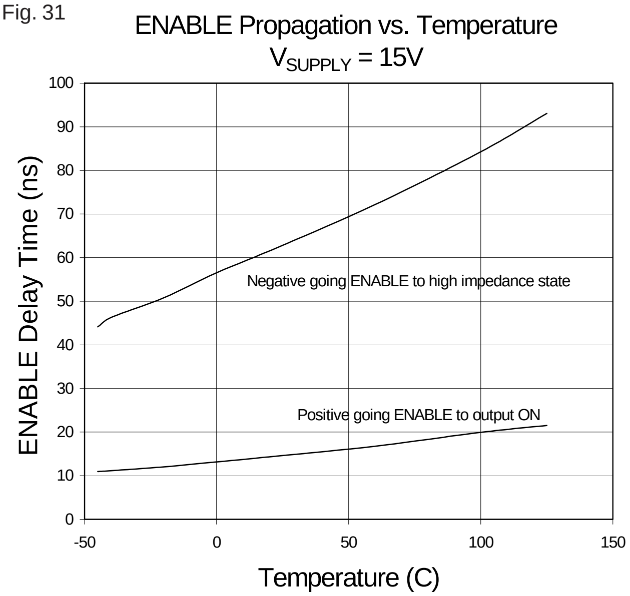
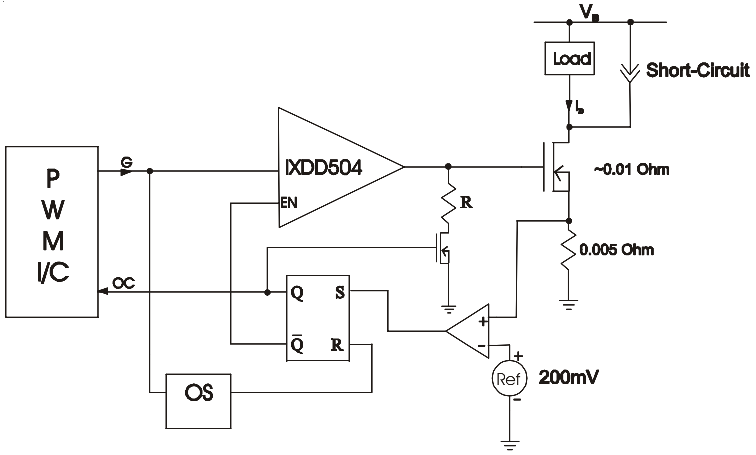


Figure 32 - Typical Application Short Circuit di/dt Limit



APPLICATIONS INFORMATION

Short Circuit di/dt Limit

A short circuit in a high-power MOSFET such as the IXFN100N20, (20A, 1000V), as shown in Figure 32, can cause the current through the module to flow in excess of 60A for 10µs or more prior to self-destruction due to thermal runaway. For this reason, some protection circuitry is needed to turn off the MOSFET module. However, if the module is switched off too fast, there is a danger of voltage transients occuring on the drain due to Ldi/dt, (where L represents total inductance in series with drain). If these voltage transients exceed the MOSFET's voltage rating, this can cause an avalanche breakdown.

The IXDD504 and IXDE504 have the unique capability, with additional circuitry, to softly switch off the high-power MOSFET module, significantly reducing these Ldi/dt transients.

Thus, the IXDD504 & IXDE504 help to prevent device destruction from *both* dangers; over-current, *and* avalanche breakdown due to di/dt induced over-voltage transients.

The IXDD504 & IXDE504 are designed to not only provide ±4A per output under normal conditions, but also to allow their outputs to go into a high impedance state. This permits the IXDD504 or IXDE504 outputs to control a separate weak pull-down circuit during detected overcurrent shutdown conditions to limit and separately control d_{VGS}/dt gate turnoff. This circuit is shown in Figure 33.

Referring to Figure 33, the protection circuitry should include a comparator, whose positive input is connected to the source of the IXFN100N20. A low pass filter should be added to the input of the comparator to eliminate any glitches in voltage caused by the inductance of the wire connecting the source resistor to ground. (Those glitches might cause false triggering of the comparator).

The comparator's output should be connected to a SRFF(Set Reset Flip Flop). The flip-flop controls both the Enable signal, and the low power MOSFET gate. Please note that CMOS 4000-series devices operate with a V_{CC} range from 3 to 15 VDC, (with 18 VDC being the maximum allowable limit).

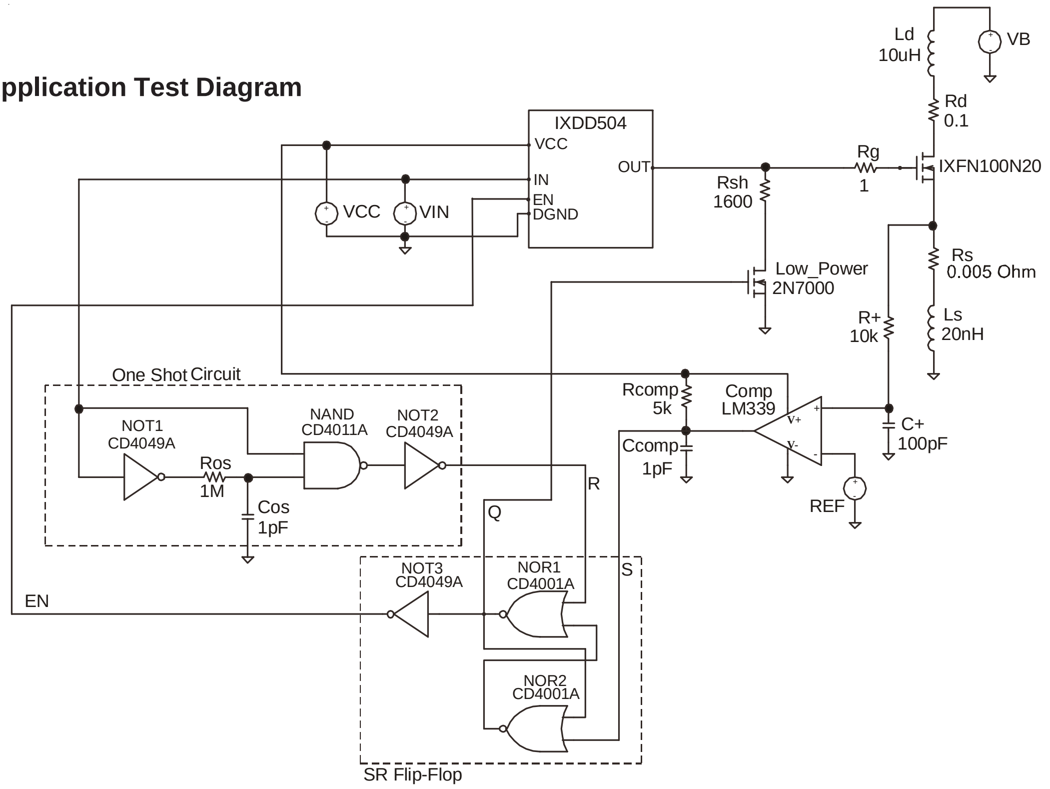
A low power MOSFET, such as the 2N7002, in series with a resistor, will enable the IXFN100N20 gate voltage to drop gradually. The resistor should be chosen so that the RC time constant will be 100us, where "C" is the Miller capacitance of the IXFN100N20.

For resuming normal operation, a Reset signal is needed at the SRFF's input to enable the IXDD504 again. This Reset can be generated by connecting a One Shot circuit between the IXDD504 Input signal and the SRFF restart input. The One Shot will create a pulse on the rise of the IXDD504 input, and this pulse will reset the SRFF outputs to normal operation.

When a short circuit occurs, the voltage drop across the low-value, current-sensing resistor, (Rs=0.005 Ohm), connected between the MOSFET Source and ground, increases. This triggers the comparator at a preset level. The SRFF drives a low input into the Enable pin disabling the IXDD504 output. The SRFF also turns on the low power MOSFET, (2N7000).

In this way, the high-power MOSFET module is softly turned off by the IXDD504, preventing its destruction.

Figure 33 - Application Test Diagram



Supply Bypassing and Grounding Practices, Output Lead inductance

When designing a circuit to drive a high speed MOSFET utilizing the IXDD504 or IXDE504, it is very important to keep certain design criteria in mind, in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, we are using the IXDD504 to charge a 2500pF capacitive load from 0 to 25 volts in 25ns.

Using the formula: $I_C = C (\Delta V / \Delta t)$, where ΔV=25V C=2500pF and Δt=25ns we can determine that to charge 2500pF to 25 volts in 25ns will take a constant current of 2.5A. (In reality, the charging current won't be constant, and will peak somewhere around 4A).

SUPPLY BYPASSING

In order for our design to turn the load on properly, the IXDD504 must be able to draw this 2.5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is a magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse current-service capacitors). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXDD504 to an absolute minimum.

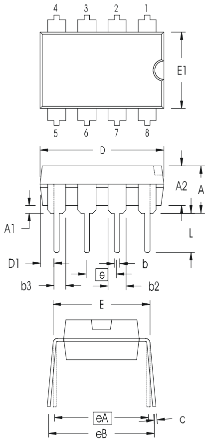
GROUNDING

In order for the design to turn the load off properly, the IXDD504 must be able to drain this 2.5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXDD504 and it's load. Path #2 is between the IXDD504 and it's power supply. Path #3 is between the IXDD504 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, (for instance), the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXDD504.

OUTPUT LEAD INDUCTANCE

Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and it's load as short and wide as possible. If the driver must be placed farther than 0.2" from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connect directly to the ground terminal of the load.

REV	DATE	ECN NO	DESCRIPTION	APR

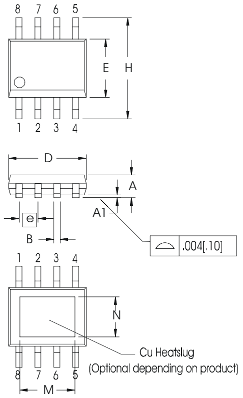


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
b3	.035	.045	0.89	1.14
c	.009	.012	0.23	0.30
D	.355	.400	9.02	10.16
D1	.010	.040	0.25	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

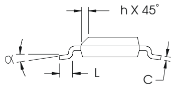
NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES
MS-001 BA.

IXYS Corp 3540 Bassett St., Santa Clara, CA 95054	TOLERANCE Unless Otherwise Specified .X=+/-.05 .XXX=+/-.005 .XX=+/-.01 ANGLE=+/-5	DATE: 8/18/94 UNIT: INCH [MM] SACLE: 4 X	DWN: K. R. Choi APR: APR:	TITLE CASE OUTLINE OF 8 LEAD 0.3"W P-DIP	DRAWING NO CO 0035	REV 0

REV	DATE	ECN NO	DESCRIPTION	APR
A	3/08/2		Added bottom heatslug dimension.	K. R. Choi



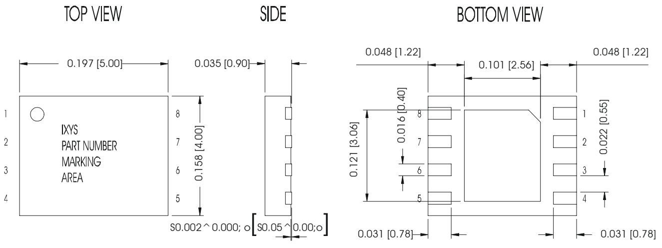
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
B	.013	.020	0.33	0.51
C	.008	.010	0.19	0.25
D	.189	.197	4.80	5.00
E	.150	.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.228	.244	5.80	6.20
h	.010	.020	0.25	0.50
L	.016	.050	0.40	1.27
M	.135	.155	3.43	3.94
N	.095	.115	2.41	2.92
α	0°	8°	0°	8°



NOTE: This drawing will meet all dimensions requirement of JEDEC MS-012 AA.

IXYS Corp 3540 Bassett St., Santa Clara, CA 95054	TOLERANCE Unless Otherwise Specified .X=+/-.05 .XXX=+/-.005 .XX=+/-.01 ANGLE=+/-5	DATE: 1/24/95 UNIT: INCH [MM] SCALE: 5X	DWN: K. R. Choi APR: APR:	TITLE CASE OUTLINE SOP-8 (.150"W)	DRAWING NO CO 0044	REV A

REV	DATE	ECN NO	DESCRIPTION	APPROVAL



IXYS Corporation 3540 BASSETT ST., SANTA CLARA, CA 95054-2704 TEL: 408-982-0700 FAX: 408-748-9788	TOLERANCE Unless Otherwise Specified .X= .010 .XXX= .002 E .XX= .005 ANGLE= 5 E °	DATE: 6/16/06 UNIT: inch [mm] SCALE: 10 X	DWN: K. R. Choi APR: FILE:	MATERIAL:	TITLE: CASE OUTLINE 8 LD DFN (4 X 5 MM 0.95MM PITCH)	DWG NO: CO 0221 SHEET NO: OF 1	REV: 0 1

IXYS Corporation
3540 Bassett St; Santa Clara, CA 95054
Tel: 408-982-0700; Fax: 408-496-0670
e-mail: sales@ixys.net
www.ixys.com

IXYS Semiconductor GmbH
Edisonstrasse15 ; D-68623; Lampertheim
Tel: +49-6206-503-0; Fax: +49-6206-503627
e-mail: marcom@ixys.de